(9) CLAIMS

1. An integrated circuit structure comprising:

a circuit die;

at least one input-output pad for connecting to said circuit die;

wafer-level packaging including an electrically conductive material beam and at least one active circuit element wherein the active circuit element integrates therein at least a segment of said beam.

2. The structure as set forth in claim 1 comprising:

said active circuit element is a resistor employing a predetermined length and geometric shape within of said beam.

3. The structure as set forth in claim 2 further comprising:

said resistor has at least two leads extending to the surface of said device and forming taps for accessing said resistor.

4. The structure as set forth in claim 1 comprising:

said beam is encased in a dielectric material, and

said active circuit element is a capacitor having a first plate formed by a predefined region of said beam.

5. The structure as set forth in claim 4 further comprising:

a grounded second plate embedded in a top level metallization layer of said die proximate said region.

6. The structure as set forth in claim 1 comprising:

said beam is encased in a dielectric material, and

said active circuit element is an inductor having at least one coil embedded in a top level metallization layer of said die wherein a segment of said beam forms a tap for said coil.

7. The structure as set forth in claim 1 comprising:

said active circuit element is an antenna.

8. A wafer-level packaged integrated circuit device comprising:

a circuit die having at least one input-output pad;

a wafer-level package including a dielectric material layer superjacent said die and a conductive material bump-out beam encapsulated in said layer and leading to a connector bump on an external surface of said dielectric material layer; and

a sense resistor integrated into said wafer-level package, using a predetermined segment of said beam as a resistor body and having a pair of

leads from said segment through said dielectric material layer to said surface.

9. A wafer-level packaged integrated circuit device comprising:

a circuit die having at least one input-output pad and a top metal layer;

a wafer-level package including a dielectric material layer superjacent said die and a conductive material beam encapsulated in said dielectric material layer and leading to a connector bump on an external surface of said dielectric material layer; and

an ESD protection capacitor integrated into said top metal layer, using a predetermined segment of said beam as a first plate and having a grounded second plate embedded in said dielectric material layer proximate said segment.

10. A wafer-level packaged integrated circuit device comprising:

a circuit die having at least one input-output pad and a top metal layer;

a wafer-level package including a dielectric material layer superjacent said die and a conductive material beam encapsulated in said dielectric material layer and leading to a connector bump on an external surface of said dielectric material layer; and

an inductor integrated into said top metal layer, having a first tap comprising a segment of said beam, a coil embedded in said top metal layer having a proximate end electrically connected to said first tap and a second distal

end electrically connecting to said circuit die.

11. A wafer-level packaged integrated circuit device comprising:

a circuit die having at least one input-output (I/O) pad;

a wafer-level package including a dielectric material layer superjacent said die and a conductive material beam encapsulated in said dielectric material layer, said beam having a first end electrically connected to said I/O pad and having a geometric shape and size forming an antenna for said die.

12. A method for fabricating an input-output (I/O) active device for an integrated circuit die having a top metal layer and using wafer-level packaging, said packaging including a dielectric material layer superjacent said die and a conductive material bump-out beam encapsulated in said layer and leading to a connector bump on an external surface of said dielectric material layer, the method comprising:

forming at least a part of said active device in a dielectric said top metal layer;

forming a segment of said beam as another integral part of said active device; and

forming an electrical connection between said part of said active device and said segment.